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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,504	10/30/2003	Takashi Naiki	12844.0050US01	8052
23552	7590	06/29/2004	EXAMINER	
MERCHANT & GOULD PC P.O. BOX 2903 MINNEAPOLIS, MN 55402-0903			WILLIAMS, ALEXANDER O	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/697,504

Applicant(s)

NAIKI, TAKASHI

Examiner

Alexander O Williams

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 2 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1 and 2 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>10/30/03</u> . | 6) <input type="checkbox"/> Other: ____. |

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Serial Number: 10/697504 Attorney's Docket #: 12844.0050US01

Filing Date: 10/30/2003; claimed foreign priority to 10/31/2002

Applicant: Naiki

Examiner: Alexander Williams

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The drawings are objected to because the related art figures should be labeled "related art."

Correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless —

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 2 are rejected under 35 U.S.C. § 102(b) as being anticipated by (Japan Patent # 4-94732).

1. (Japan Patent # 4-94732) show a semiconductor integrated circuit device **1** having bumps **3**, which are used for electrically connecting by face down bonding and provided in a terminal section on a surface of a semiconductor substrate thereof, said semiconductor integrated circuit device further comprising: facedown bonding dummy bumps **5** which are connected non-electrically and disposed in a vicinity of one or more corner sections of four corners of a semiconductor chip, wherein an area of each of said facedown bonding dummy bumps projected onto a chip is larger than that of the area of each said facedown bonding bumps.
2. The semiconductor integrated circuit device according to claim 1, (Japan Patent # 4-94732) wherein said dummy bumps **5** are functioning as shock absorbing members for alleviating load stress due to the facedown bonding, and are not electrically connected to a wiring of which part is disposed to be overlapped to said facedown bonding dummy bumps with at least one insulating film being interposed in-between.

Claims 1 and 2 are rejected under 35 U.S.C. § 102(b) as being anticipated by (Japan Patent # 8-46313).

1. (Japan Patent # 8-46313) show a semiconductor integrated circuit device **2** having bumps **4**, which are used for electrically connecting by face down bonding and provided in a terminal section on a surface of a semiconductor substrate thereof, said semiconductor integrated circuit device further comprising: facedown bonding dummy bumps **10** which are connected non-electrically and disposed in a vicinity of one or more

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corner sections of four corners of a semiconductor chip, wherein an area of each of said facedown bonding dummy bumps projected onto a chip is larger than that of the area of each said facedown bonding bumps.

2. The semiconductor integrated circuit device according to claim 1, (Japan Patent # 8-46313) wherein said dummy bumps **10** are functioning as shock absorbing members for alleviating load stress due to the facedown bonding, and are not electrically connected to a wiring of which part is disposed to be overlapped to said facedown bonding dummy bumps with at least one insulating film being interposed in-between.

Claims 1 and 2 are rejected under 35 U.S.C. § 102(e) as being anticipated by Yagi et al. (Japan Patent # 2003-282812).

1. Yagi et al. (figures 1a to 5b) specifically figure 1 a show a semiconductor integrated circuit device having bumps **11**, which are used for electrically connecting by face down bonding and provided in a terminal section on a surface of a semiconductor substrate thereof, said semiconductor integrated circuit device further comprising: facedown bonding dummy bumps **15** which are connected non-electrically and disposed in a vicinity of one or more corner sections of four corners of a semiconductor chip, wherein an area of each of said facedown bonding dummy bumps projected onto a chip is larger than that of the area of each said facedown bonding bumps .

2. The semiconductor integrated circuit device according to claim 1, Yago et al. show wherein said dummy bumps are functioning as shock absorbing members for alleviating load stress due to the facedown bonding, and are not electrically connected to a wiring of which part is disposed to be overlapped to said facedown bonding dummy bumps with at least one insulating film being interposed in-between.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Claims 1 and 2 are rejected under 35 U.S.C. § 102(b) as being anticipated by (Japan Patent # 9-115910).

1. (Japan Patent # 9-115910) show a semiconductor integrated circuit device **21** having bumps **11**, which are used for electrically connecting by face down bonding and provided in a terminal section on a surface of a semiconductor substrate thereof, said

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semiconductor integrated circuit device further comprising: facedown bonding dummy bumps **9** which are connected non-electrically and disposed in a vicinity of one or more corner sections of four corners of a semiconductor chip, wherein an area of each of said facedown bonding dummy bumps projected onto a chip is larger than that of the area of each said facedown bonding bumps .

2. The semiconductor integrated circuit device according to claim 1, (Japan Patent # 9-115910) show wherein said dummy bumps **9** are functioning as shock absorbing members for alleviating load stress due to the facedown bonding, and are not electrically connected to a wiring of which part is disposed to be overlapped to said facedown bonding dummy bumps with at least one insulating film being interposed in-between.

Claims 1 and 2 are rejected under 35 U.S.C. § 102(b) as being anticipated by Sato (U.S. Patent # 6,287,895 B1).

1. Sato (figures 1A to 9) specifically figure 7 show a semiconductor integrated circuit device **17** having bumps **13**, which are used for electrically connecting by face down bonding and provided in a terminal section on a surface of a semiconductor substrate thereof, said semiconductor integrated circuit device further comprising: facedown bonding dummy bumps **12** which are connected non-electrically and disposed in a vicinity of one or more corner sections of four corners of a semiconductor chip, wherein an area of each of said facedown bonding dummy bumps projected onto a chip is larger than that of the area of each said facedown bonding bumps .

2. The semiconductor integrated circuit device according to claim 1, Sato show wherein said dummy bumps **12** are functioning as shock absorbing members for alleviating load stress due to the facedown bonding, and are not electrically connected to a wiring of which part is disposed to be overlapped to said facedown bonding dummy bumps with at least one insulating film being interposed in-between.

The following references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/737,738,734,778,780,781,784,772,775	6/28/04
Other Documentation: foreign patents and literature in 257/737,738,734,778,780,781,784,772,775	6/28/04
Electronic data base(s): U.S. Patents EAST	6/28/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
6/28/04



Primary Patent Examiner
Alexander O. Williams